WHAT IS CLAIMED IS:

1. A method for reducing current in a semiconductor memory device comprising a plurality of rows of memory cells, the method comprising:

maintaining a plurality of bits indicative of rows of memory cells that are to be refreshed; and

refreshing only those rows that are to be refreshed, as indicated by the plurality of bits.

2. The method of claim 1, further comprising:

obtaining an indication of a limited portion of the plurality of rows to be included in refresh operations; and

only refreshing those rows both indicated by the bits and contained in the limited portion.

3. The method of claim 2, wherein receiving an indication of the limited portion comprises reading a partial array refresh mode register.

4. The method of claim 1, wherein maintaining a plurality of bits indicative of rows of memory cells that are to be refreshed comprises:

monitoring write operations; and

setting bits corresponding to rows of data involved in the monitored write operations.

5. The method of claim 4, further comprising only clearing bits corresponding to rows of data involved in the monitored write operations in response to a reset event.

6. The method of claim 5, wherein the reset event is indicated by a mode register.

7. A method for selectively refreshing rows of memory cells in one or more semiconductor memory devices, comprising:

monitoring write operations to memory cells;

maintaining a plurality of bits indicative of rows containing memory cells involved in the monitored write operations; and

limiting a number of rows for which refresh operations are performed based on the plurality of bits.

8. The method of claim 7, wherein limiting the number of rows for which refresh operations are performed based on the plurality of bits comprises performing refresh operations for only those rows containing memory cells involved in the monitored write operations.

9. The method of claim 7, wherein monitoring write operations to memory cells comprises monitoring the write operations by a semiconductor memory device.

10. The method of claim 7, wherein monitoring write operations to memory cells comprises monitoring the write operations by a memory controller coupled with the semiconductor memory device.

11. The method of claim 10, further comprising:

maintaining a plurality of bits indicative of rows containing memory cells involved in the monitored write operations on the memory controller;

transferring a first plurality of the bits to a first memory device; and

placing the first memory device in a self-refresh mode, in which refresh operations are performed for only those rows containing memory cells involved in the monitored write operations, as indicated by the first plurality of bits.

12. The method of claim 11, further comprising:

transferring a second plurality of the bits to a second memory device; and

placing the second memory device in a self-refresh mode, in which refresh operations are performed for only those rows containing memory cells involved in the monitored write operations, as indicated by the second plurality of bits.

13. A semiconductor memory device, comprising:

a plurality of rows of memory cells;

refresh circuitry configured to issue refresh requests for the rows of memory cells when the memory device is placed in a self-refresh mode;

row state circuitry configured to maintain a plurality of bits indicative of rows that are to be refreshed; and

refresh enable circuitry configured to limit the number of rows for which refresh requests are issued based on the bits of the row state circuitry.

14. The semiconductor memory device of claim 13, wherein the refresh enable circuitry is configured to limit the number of rows for which refresh requests are issued by generating a signal used to inhibit refresh requests.

15. The semiconductor memory device of claim 14, wherein the signal is generated by accessing a bit corresponding to a row address generated by a refresh address counter.

16. The semiconductor memory device of claim 13, wherein:

the row state circuitry is configured to set bits to indicate rows of memory cells that have been written to; and

the refresh enable circuitry is configured to limit the number of rows for which refresh requests are issued to rows that have been written to, as indicated by the bits.

17. The semiconductor memory device of claim 16, wherein each bit corresponds to a single row of memory cells.

18. The semiconductor memory device of claim 16, wherein the row state circuitry is configured to set bits to indicate rows of memory cells that have been written.

19. The semiconductor memory device of claim 18, wherein the row state circuitry is configured to maintain the set bits until the occurrence of a reset event.

19. The semiconductor memory device of claim 13, wherein the row state circuitry comprises an array of memory cells, each to store a bit indicating whether one or more memory cells of a corresponding row have been written to.

20. A system, comprising:

a memory device having a plurality of rows of memory cells, wherein the memory device is configured to limit the number of rows that are refreshed, during a self-refresh mode, based on row data indicative of rows that are to be refreshed; and

a memory controller configured to monitor write operations to the memory device, generate the row data based on the monitored write operations, and transfer the row data to the memory device prior to placing the memory device in the self-refresh mode.

21. The system of claim 20, wherein:

the row data is stored in the memory device in an array of memory cells; and

the memory controller is further configured to reset the array of memory cells prior to transferring the row data to the memory device.

22. The system of claim 21, wherein the memory controller is configured to reset the array of memory cells by writing to a mode register of the memory device.

23. The system of claim 20, wherein the memory controller is configured to set a bit in the row data to indicate one or more cells in a corresponding row have been written.